Specification Objections

The specification was objected to because of minor informalities. Applicant respectfully requests that the Examiner enter the above referenced corrections to the specification. These corrections repair previously undetected informalities as well as those pointed out by the Examiner.

Drawing Objections

Accompanying this response to the Office Action is a request to approve drawing changes. The changes provided therein contain only modifications required to correct the informalities detected by the Examiner. Applicants respectfully request that the Examiner enter these changes to the drawings.

Claim Objections

The claims were objected to because of minor informalities. Applicant respectfully requests that the Examiner enter the above referenced corrections to the claims. These corrections repair previously undetected informalities as well as those informalities pointed out by the Examiner.

Claim Rejections

35 U.S.C. §103

In the Office Action, claims 1-24 were rejected under 35 U.S.C. 103.

Sample in view of Agrawal

In the Office Action, claims 1-6 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent 6,289,494 to Sample et al. (hereinafter *Sample*) in view of U.S. Patent No. 5,644,496 to Agrawal et al. (hereinafter *Agrawal*) (Examiners Response A). For the reasons stated below Applicants respectfully submit that claims 1-6 are patentable over *Sample* in view of *Agrawal*.

Claim 1 reads:

> A crossbar device comprising:
> n input lines;
> m output lines; and
> a plurality of chains of pass transistors, each chain having a plurality of pass transistors, to selectively couple said n input lines to said m output lines;
> where n and m are integers.

In contrast, the *Sample* and *Agrawal* references simply disclose the two prior art models discussed in the background section, neither of which individually nor the two in combination discloses a plurality of chains of pass transistors each having a plurality of pass transistors, to selectively couple input lines to output lines.

Specifically, *Agrawal* merely discloses a single programmable pass transistor for connecting primary inputs (I) to long lines (LL). The programmable interconnect switches (PIPs), illustrated in Figure 2A of *Agrawal* and used to connect the primary inputs to long lines, are the same architecture as the programmable interconnect of the

prior art described in Figure 1b of the present invention. Specifically, memory cell **36** in *Agrawal*'s PIP provides a single pass transistor **35** for connecting a primary input of the I/O buffer to the long lines of the adjacent bus (Figure 6A and column 12, lines 58-63 for the I/O cell description and Figure 2A and column 7, lines 46-61 for the PIP description). Thus, *Agrawal* does not disclose a **plurality of chains of pass transistors each having a plurality of pass transistors**, to selectively couple input lines to output lines.

Sample discloses (Figure 13D) a hybrid between a fully decoded crosspoint-type crossbar and a fully encoded multiplexer-type crossbar (this is the same architecture as the prior art discussed with respect to Figure 2 in the present invention). In *Sample*, the number of programmable memory cells needed to program the device is greatly reduced compared to a fully decoded crosspoint. However, in the hybrid crossbar provided by *Sample*, there is no disclosure or suggestion related to a **plurality of chains of pass transistors, each having a plurality of pass transistors** to selectively couple input lines to output lines.

Both of the architectures disclosed in *Sample* and *Agrawal* allow for the programmable connection of signals. Indeed, both the PIP of *Agrawal* and the hybrid design of *Sample* are alternative architectures for interconnecting signals. Assuming, arguendo, that combining the two references would result in the architecture of the present invention, there is no incentive to combine the two references, especially in light of the fact that they are alternative architectures for performing the same task. Absent any discussion or suggestion to combine benefits of each of the architecture, there cannot be said to be any incentive to combine these references. Thus, Applicants respectfully submit that claim 1 is patentable over *Sample* in view of *Agrawal*.

Claims 2-6 depend from independent claim 1 incorporating its limitations. Thus, by virtue of at least their dependency on claim 1, claims 2-6 also recite patentable subject matter.

Sample in view of Patel and Admitted Prior Art

In the Office Action, claims 7, 13 and 14 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Sample* in view of Applicants' admitted prior art and U.S. Patent No. 6,175,952 to Patel et al. (hereinafter *Patel*). For the reasons stated below Applicants respectfully submit that claims 7, 13 and 14 are patentable over *Sample* in view of *Patel* and admitted prior art.

Claim 7 reads:

> A reconfigurable circuit comprising:
> a plurality of crossbar devices coupled to one another, each crossbar device having at least a memory element, and an output buffer electrically associated with the memory element; and
> a voltage supply structure coupled to the crossbar device designed to supply Vdd to the output buffers, and a voltage raised by a threshold over Vdd to the memory elements to maintain the input voltage of the output buffers at Vdd.

Sample and the admitted prior art does not teach a voltage supply structure as recited in the claim.

In *Patel*, the disclosure in Figure 23 illustrates the use of separate supply voltage in isolation device **2315** to protect circuitry connected to the output of isolation device **2315**. The protected circuitry uses VCC1. The isolation device uses VCC2. The isolation device is intended to prevent high voltages from damaging circuitry that would otherwise be driven by the signal driving the isolation device **2321** (column 26, lines 39-

42). A specific example of the usage of this isolation device is discussed in Figure 10A and related Figures 8 and 9. This discussion in *Patel* is related to the handling of connection of I/O pins which are connect to other devices that may have different voltage levels from that of the I/O pin (e.g. where a 3.3 volt I/O pin is connected to a 5 volt device, column 10 lines 27-37). Thus, the cited sections in column 13 describe how the circuitry of the voltage bias generator **1002** will operate to protect the circuitry if a voltage higher then VCC+VTP (supply voltage plus a threshold voltage) is driven on the pin **820**. There is no discussion relating to a voltage raised by a threshold over Vdd to the memory elements **to maintain the input voltage of the output buffers at Vdd**. Thus, assuming arguendo, that there is motivation to combine *Sample* and *Patel*, the resulting circuitry would not result in a voltage raised by a threshold over Vdd to the memory elements **to maintain the input voltage of the output buffers at Vdd**. Thus, Applicants respectfully submit that claim 7 is patentable over *Sample* in view of *Patel* and admitted prior art.

Claims 13-14 depend from independent claim 7 incorporating its limitations. Thus, by virtue of at least their dependency on claim 7, claims 13-14 also recite patentable subject matter.

Sample in view of Patel, Agrawal and Admitted Prior Art

In the Office Action, claims 8-12 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Sample* in view of Applicants' admitted prior art, *Patel* and *Agrawal*. For the reasons stated below Applicants respectfully submit that claims 8-12 are patentable over *Sample* in view of *Patel, Agrawal* and admitted prior art.

Claims 8-12 depend from claim 7. In addition to the limitations of claim 7, these claims contain additional limitations substantially similar to claim 1. *Patel* does not solve the deficiencies of the previous arguments with respect to claim 1. In addition, *Agrawal* does not solve the deficiencies of the previous arguments with respect to claim 7. Thus, for at least the reasons set forth with respect to both claim 1 and claim 7 above, Applicants respectfully submit that claims 8-12 are patentable over *Sample* in view of admitted prior art, *Patel* and *Agarwal*.

Sample in view of Burstein and Admitted Prior Art

In the Office Action, claims 15, 16, 23 and 24 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Sample* in view of Applicants' admitted prior art and U.S. Patent No. 5,744,990 to Burstein (hereinafter *Burstein)*. For the reasons stated below, Applicants respectfully submit that claims 15, 16, 23 and 24 are patentable over *Sample* in view of *Burstein* and admitted prior art.

Claim 15, as amended, reads:

> A reconfigurable circuit comprising:
> a plurality of crossbar devices coupled to one another, each crossbar device having at least an output buffer; and
> a power-on circuitry coupled to the crossbar devices to force the output buffers to a known logic value at power-on.

Thus, in the present invention, the output buffers of a crossbar device are forced to a known logic value. The benefit of such forcing to a known logic value is to prevent large current draws and, resultantly, potential damage to the crossbar device. In contrast, *Burstein*, and traditional Power-on-Reset (POR) usage, are concerned with the

setting of sequential and clocking devices to known states to provide predictability in the function of such circuits upon recovery from reset.

In addition, there is no motivation to combine the POR circuitry of *Burstein* in a crossbar device of *Sample*. There is no disclosure or suggestion in *Burstein* to use the POR circuitry in a crossbar circuit to prevent large current draws and, resultantly, potential damage to the crossbar device. Absent some motivation to combine the references, a rejection based on a combination of references is improper.

Thus, for at least the reasons discussed above, Applicants respectfully submit that claim 15 is patentable over *Sample* in view of the admitted prior art and *Burstein*. Claims 16, 22 and 23 depend from claim 15. Thus, for at least the reasons discussed above with respect to claim 15, Applicants respectfully submit that claims 16, 22 and 23 are patentable over *Sample* in view of the admitted prior art and *Burstein*.

Sample in view of Agrawal, Burstein and Admitted Prior Art

In the Office Action, claims 17-21 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Sample* in view of *Agrawal*, *Burstein* and Applicants' admitted prior art. For the reasons stated below, Applicants respectfully submit that claims 17-21 are patentable over *Sample* in view of *Agrawal*, *Burstein*, and Applicants' admitted prior art.

Claims 17-21 depend from claim 15. In addition to the limitations of claim 15, these claims contain additional limitations substantially similar to claim 1. *Burstein* does not solve the deficiencies of the previous arguments with respect to claim 1. In addition, *Agrawal* does not solve the deficiencies of the previous arguments with respect to claim

15. *Thus*, Applicants respectfully submit that, for at least the same reasons discussed above with respect to both claims 1 and 15, claims 17-21 are patentable over *Sample* in view of *Agrawal*, *Burstein* and Applicants' admitted prior art.

Sample in view of Burstein, Patel and Admitted Prior Art

In the Office Action, claim 22 was rejected under 35 U.S.C. §103(a) as being unpatentable over *Sample* in view of *Burstein*, *Patel* and Applicants' admitted prior art. For the reasons stated below, Applicants respectfully submit that claim 22 is patentable over *Sample* in view of *Burstein*, *Patel* and Applicants' admitted prior art.

Claim 22 depends from claim 15. In addition to the limitations of claim 15, claim 22 contain additional limitations substantially similar to claim 7. *Burstein* does not solve the deficiencies of the previous arguments with respect to claim 7. In addition, *Patel* does not solve the deficiencies of the previous arguments with respect to claim 15. Thus, Applicants respectfully submit that, for at least the same reasons discussed above with respect to both claims 15 and 7, claim 22 is patentable over *Sample* in view of *Burstein*, *Patel* and Applicants' admitted prior art.

Conclusion

In view of the forgoing, Applicants respectfully submit that claims 1-24 are in condition for allowance. Early issuance of the Notice of Allowance is respectfully requested.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393. A Fee Transmittal is enclosed in duplicate for fee processing purposes.

Respectfully submitted,
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Appendix A - VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Paragraph beginning at page 3, line 20 has been amended as follows:

Figure 3 shows another prior art implementation (US PAT 5.260.610). This type of crossbar also needs (n / 2) x m memory elements **301** plus m memory elements **302**. To connect input line **303a** to output line **304** we must program a 1 in memory element **301** and a 1 in memory element **302**. But, by programming a one in memory element **301**, input line **303b** is connected to capacitance **306**. Capacitance **306** is large because it represents the parasitic load of half of the pass transistor of one column plus the metal interconnection between them. If the crossbar has 32 inputs, then capacitance **306** includes the parasitic load of 16 n-mos drains/sources. Again, the capacitive loading of one input lines can vary dramatically with the programming pattern of the other inputs.

Paragraph beginning at page 4, line 4 has been amended as follows:

In applications where a significant number of crossbars are employed and interconnected, such as reconfigurable circuit applications, the input capacitive load variation of one crossbar input with respect to the programming pattern of its other inputs makes the timing optimization of high performance devices very difficult. Additionally, these and other prior art crossbar devices are found to consume more power and/or area than desired, as well as contributing to current swing.

Paragraph beginning at page 5, line 16 has been amended as follows:

In accordance with another aspect, a low power application of multiple crossbar devices to a reconfigurable circuit block is improved by having each memory element of a crossbar device be provided with a supply voltage higher by a threshold voltage Vth to maintain the supply voltage of corresponding output buffers input at Vdd, to prevent the output buffers from consuming static current when their inputs are at a ~~degenrated~~degenerated level, to facilitate the lower power application.

Paragraph beginning at page 9, line 8 has been amended as follows:

As alluded to earlier, employing crossbar devices in a low power manner is especially desirable for an integrated circuit or integrated circuit block where a significant number of crossbar devices are employed and interconnected. An example of such integrated circuit is the scalable reconfigurable circuit disclosed in co-pending U.S. Patent Application, number 09/971,349~~<to be inserted>~~, entitled "A Reconfigurable Integrated Circuit Having a Scalable Architecture", filed 10/4/2001~~<to be inserted>~~, having common inventorship with present application. The specification of which is hereby fully incorporated by reference.

Paragraph beginning at page 9, line 20 has been amended as follows:

Figure 7 shows an improved crossbar output buffer structure to avoid static current at power-up, in accordance with yet another aspect of the present invention. As mentioned above, at power-up, the state of the memory elements are undefined. This

may create various paths between the inputs of a crossbar. For a reconfigurable circuit block, such as the one disclosed in co-pending application '349~~123~~, many output buffers may be shorted together at power-up, producing a large current flow through the device. Also, during configuration loading sequence of the circuit block, the incomplete configuration may ~~temporary~~ create temporary short circuits between the crossbar inputs. To compensate for these possibilities, the output buffers **704** are advantageously connected to a global control line **701** forcing their outputs to a known level. This control line is activated by a power-on reset circuitry **702** and is ~~desactivated~~deactivated when a configuration has been loaded in the reconfigurable circuit block. Since all the crossbar outputs are at the same level during the power-up and until a configuration is loaded, the fact that they may or may not be shorted together does not produce any more current. For example, at power up, power on reset circuitry **702** resets the flip-flop **703**. The flip-flop output **701** forces all the crossbar buffers **704** to zero. When a configuration is loaded, flip flop **702** is written with a logical 1, enabling all crossbar output buffers.

In the Claims

Marked up versions of the amended claims follow.

1. (Once Amended) A crossbar device comprising:

n input lines;

m output lines; and

a plurality of chains of pass transistors, each chain having a plurality of pass transistors, to ~~seletively~~selectively couple said n input lines to said m output lines;

where n and m are integers.

2. (Once Amended) The crossbar device of claim 1, wherein at least one of the plurality of chains of pass transistors consists of a first and a second pass ~~transitor~~transistor.

3. (Once Amended) The crossbar device of claim 1, wherein each of the plurality of chains of pass transistors consists of a first and a second pass ~~transitor~~transistor.

5. (Once Amended) The crossbar device of claim 1, wherein the device further comprises a plurality of p to q decoder logics coupled to the input lines, where p and q are integers, with p being less than q.

7. (Once Amended) A reconfigurable circuit comprising:

a plurality of crossbar devices coupled to one another, each crossbar device having at least a memory element, and an output buffer electrically ~~assocaited~~associated with the memory element; and

a voltage supply structure coupled to the crossbar device designed to supply Vdd to the output buffers, and a voltage raised by a threshold over Vdd to the memory elements to maintain the input voltage of the output buffers at Vdd.

8. (Once Amended) The reconfigurable circuit of claim 7, wherein at least one of the plurality of crossbar devices ~~comrpises~~comprises

n input line;

m output lines; and

a plurality of chains of pass transistors coupling the n input lines to the m output lines;

where n and m are integers.

9. (Once Amended) The reconfigurable circuit of claim 8, wherein at least one of the plurality of chains of pass transistors consists of a first and a second pass ~~transitor~~transistor.

10. (Once Amended) The reconfigurable circuit of claim 8, wherein each of the plurality of chains of pass transistors consists of a first and a second pass ~~transitor~~transistor.

11. (Once Amended) The reconfigurable circuit of claim 7, wherein each of the plurality of crossbar devices ~~comrpises~~comprises:

n input line;

m output lines; and

a plurality of chains of pass transistors coupling the n input lines to the m output lines;

where n and m are integers.

15. (Once Amended) A reconfigurable circuit comprising:

a plurality of crossbar devices coupled to one another, each crossbar device having at least an output buffer; and

a power-on circuitry coupled to the crossbar devices to force the output buffers to a known ~~state~~ logic value at power-on.

17. (Once Amended) The reconfigurable circuit of claim 15, wherein at least one of the plurality of crossbar devices ~~comrpises~~comprises:

n input line;

m output lines; and

a plurality of chains of pass transistors coupling the n input lines to the m output lines;

where n and m are integers.

18. (Once Amended) The reconfigurable circuit of claim 17, wherein at least one of the plurality of chains of pass transistors consists of a first and a second pass ~~transitor~~transistor.

19. (Once Amended) The reconfigurable circuit of claim 17, wherein each of the plurality of chains of pass transistors consists of a first and a second pass ~~transitor~~transistor.

20. (Once Amended) The reconfigurable circuit of claim 15, wherein each of the plurality of crossbar devices ~~comrpises~~comprises:

n input line;

m output lines; and

a plurality of chains of pass transistors coupling the n input lines to the m output lines;

where n and m are integers.

22. (Once Amended) The reconfigurable circuit of claim 15, wherein

each crossbar device further having at least a memory element electrically associated to an output buffer; and

the reconfigurable ~~circuitr~~circuit further ~~comprisees~~comprises a voltage supply structure coupled to the crossbar devices designed to supply Vdd to the output buffers, and a voltage raised by a threshold over Vdd to the memory elements to maintain the voltage supply of the output buffers at Vdd.